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PLUS Search Results for S/N 10602581, Searched November 16, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated sear ch

system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that a re

most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

## 10602581\_LIST

5	5	5	7	7	5	7	
5	5	6	8	6	2	1	
5	5	8	7	9	2	1	
5	6	4	4	4	9	6	
5	7	4	2	1	8	1	
5	8	2	6	0	4	8	
5	9	7	0	2	3	4	
6	1	8	1	1	6	6	
4	8	5	1	9	9	0	
5	2	1	2	6	5	2	
5	2	3	3	5	3	9	
5	2	6	0	8	8	1	
5	3	2	9	4	6	0	
5	3	5	9	5	3	6	
5	4	2	2	8	2	3	

## 10602581\_QUAL

6272601	61
6275906	61
6338121	61
6389516	61
6430658	61
6460133	61
6763415	56
6785758	56
6813673	56
6100715	54
6204686	54
6434735	54
6287765	54
5809322	54
5974521	54
6460127	54
6463553	54
5784636	52
4367524 5632029	52 50 50
5685004	50
5978880	50
5428811	50
5438670 6032229	50 50 50
5465344	50
5524175	50
6107818	50
6427156	50
5517650	50
6157205	50
5440182	50
6000051	50
6021483	50
5455521	50
5557757	50
5568621	50
5587921	50
5644496	50
5742181	50
5826048	50
5970234	50
6181166	50
4851990	50
4851990 5212652 5233539	50 50
5260881	50
5329460	50

## 10602581\_QUAL

5359536 50 5422823 50

#### 10602581 CLS

Most Frequently Occurring Classifications of Patents Returned From A Search of 10602581 on November 16, 2004

#### 3 710/305 2 326/39 2 326/41 2 710/306 2 710/316 2 711/140 2 711/146 Cross-Reference Classifications 6 326/41 6 716/17 4 326/39 4 708/232 3 340/14.3 3 710/107 2 326/38 2 326/86 2 340/2.2 2 710/309 2 711/133 2 712/19 Combined Classifications 8 326/41 7 716/16 7 716/17 6 326/39 4 708/232 3 326/38 3 340/14.3 3 710/107 3 710/305 3 711/146 2 326/17 2 326/83 2 326/86 2 340/2.2 2 710/240 2 710/306 2 710/309 2 710/316 2 711/133

Original Classifications

7 716/16

### 10602581\_CLS

- 711/140
- 712/11 712/14
- 712/19

- 2 2 2 2 2 2 712/214 712/23 712/37

#### 10602581 CLSTITLES

Titles of Most Frequently Occurring Classifications of Patents Returne d

From A Search of 10602581 on November 16, 2004

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8
 326/41
               (2 OR, 6 XR)
       Class 326: ELECTRONIC DIGITAL LOGIC CIRCUITRY
                     MULTIFUNCTIONAL OR PROGRAMMABLE (E.G.,
       326/37
                          UNIVERSAL, ETC.)
                     .Array (e.g., PLA, PAL, PLD, etc.)
       326/39
                     .. Significant integrated structure, layout, or
       326/41
                        layout interconnections
7 716/16
               (7 \text{ OR}, 0 \text{ XR})
               716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
       Class
                       CIRCUIT OR SEMICONDUCTOR MASK
                     CIRCUIT DESIGN
       716/1
       716/12
                     .Routing (e.g., routing map, netlisting)
                     ..PLA, PLD, FPGA, OR MCM
        716/16
7 716/17
               (1 OR, 6 XR)
       Class 716: DATA PROCESSING: DESIGN AND ANALYSIS OF
                       CIRCUIT OR SEMICONDUCTOR MASK
                     CIRCUIT DESIGN
        716/1
       716/17
                     .Programmable integrated circuit (e.g., basic
                        cell, standard cell, macrocell)
6 326/39
               (2 OR, 4 XR)
        Class 326: ELECTRONIC DIGITAL LOGIC CIRCUITRY
                     MULTIFUNCTIONAL OR PROGRAMMABLE (E.G.,
        326/37
                         UNIVERSAL, ETC.)
                      .Array (e.g., PLA, PAL, PLD, etc.)
        326/39
               (0 OR, 4 XR)
   708/232
               708 : ELECTRICAL COMPUTERS: ARITHMETIC PROCESSING
        Class
                       AND CALCULATING
                    ELECTRICAL DIGITAL CALCULATING COMPUTER
        708/100
                    .Particular function performed
        708/200
        708/230
                     ..Multifunctional
                     ... Array of elements (e.g., AND/OR array, etc.
        708/232
   326/38
                (1 OR, 2 XR)
                326 : ELECTRONIC DIGITAL LOGIC CIRCUITRY
        Class
                     MULTIFUNCTIONAL OR PROGRAMMABLE (E.G.,
        326/37
                         UNIVERSAL, ETC.)
                      .Having details of setting or programming of
        326/38
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# 10602581\_CLSTITLES interconnections or logic functions

3	340/825 340/14.1	340	OR, 3 XR) : COMMUNICATIONS: ELECTRICAL SELECTIVE .Decoder matrixProgrammable
3	710/100	710	OR, 3 XR) : ELECTRICAL COMPUTERS AND DIGITAL DATA     PROCESSING SYSTEMS: INPUT/OUTPUT     INTRASYSTEM CONNECTION (E.G., BUS AND BUS         TRANSACTION PROCESSING) .Bus access regulation
3	Class 710/100	710	OR, 0 XR) : ELECTRICAL COMPUTERS AND DIGITAL DATA     PROCESSING SYSTEMS: INPUT/OUTPUT INTRASYSTEM CONNECTION (E.G., BUS AND BUS     TRANSACTION PROCESSING) .Bus interface architecture
3	711/100	711	: ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY STORAGE ACCESSING AND CONTROL .Hierarchical memoriesCachingCoherency
2		326	OR, 1 XR) : ELECTRONIC DIGITAL LOGIC CIRCUITRY ACCELERATING SWITCHING
2	326/83 Class 326/62 326/82 326/83	(1 326	OR, 1 XR) : ELECTRONIC DIGITAL LOGIC CIRCUITRY INTERFACE (E.G., CURRENT DRIVE, LEVEL SHIFT, ETC.) .Current driving (e.g., fan in/out, off chip driving, etc.)Field-effect transistor
2			OR, 2 XR) : ELECTRONIC DIGITAL LOGIC CIRCUITRY INTERFACE (E.G., CURRENT DRIVE, LEVEL SHIFT, ETC.) .Current driving (e.g., fan in/out, off chip

# 10602581\_CLSTITLES driving, etc.)

	326/83 326/86		driving, etc.)Field-effect transistorBus driving
2	340/825 340/2.1	340	OR, 2 XR) : COMMUNICATIONS: ELECTRICAL SELECTIVE .Path selectionChannel selecting matrix
2		710	OR, 1 XR) : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT ACCESS ARBITRATING
2		710	: ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING) .Bus interface architecture
2	710/309	(0 710	OR, 2 XR) : ELECTRICAL COMPUTERS AND DIGITAL DATA     PROCESSING SYSTEMS: INPUT/OUTPUT     INTRASYSTEM CONNECTION (E.G., BUS AND BUS
2	710/316 Class 710/100 710/305 710/316	710	OR, 0 XR) : ELECTRICAL COMPUTERS AND DIGITAL DATA     PROCESSING SYSTEMS: INPUT/OUTPUT     INTRASYSTEM CONNECTION (E.G., BUS AND BUS
2	711/133 Class 711/100 711/117 711/118 711/133	711	OR, 2 XR) : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING     SYSTEMS: MEMORY     STORAGE ACCESSING AND CONTROL     .Hierarchical memories    Caching    Entry replacement strategy

2	711/140 Class 711/100 711/117 711/118 711/140	711	10602581_CLSTITLES OR, 0 XR) : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING    SYSTEMS: MEMORY STORAGE ACCESSING AND CONTROL .Hierarchical memoriesCachingCache pipelining
2			OR, 1 XR) : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INS
TRUC	TION		PROCESSING
	712/1 712/10 712/11		
2	712/14 Class		OR, 1 XR) : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INS
TRUC	TION		PROCESSING
	712/1 712/10 712/11 712/14		PROCESSING ARCHITECTURE .Array processorArray processor element interconnectionProcessing element memory
2	712/19 Class		
TRUC	712/1 712/10 712/16 712/19		PROCESSING PROCESSING ARCHITECTURE .Array processorArray processor operationSystolic array processor
2	712/214 Class		OR, 1 XR) : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INS
TRUC	712/214		PROCESSING INSTRUCTION ISSUING
2	712/23 Class		OR, 1 XR) : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INS
TRUC	TION		

### 10602581\_CLSTITLES

PROCESSING

712/1 PROCESSING ARCHITECTURE 712/23 .Superscalar

2 712/37 (1 OR, 1 XR)

Class 712: ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND IN

TRUCTION

PROCESSING

712/1 PROCESSING ARCHITECTURE

712/32 .Microprocessor or multichip or multimodule

processor having sequential program contro

1

712/37 ..Programmable (e.g., EPROM)